Remarks

Claims 1-31 are pending in the current application. Claims 1, 14-17 and 24 have been amended. Claims 5 and 27 have been canceled.

Indication of Allowable Subject Matter

Claims 4, 16-19, 21-23, 29 and 30 stand objected to as being dependent upon a rejected base claim, but are indicated as allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants thank the Examiner for the indication of allowable subject matter.

35 U.S.C. 102 Rejections

Claims 1-3 and 5-13 have been rejected under 35 U.S.C. 102(e) as being anticipated by Pekny, U.S. Pat. No. 6,553,510.

Claims 14-15 have been rejected under 35 U.S.C. 102(e) as being anticipated by Scheuerlein et al., "Scheuerlein," U.S. Pat. No. 6,868,022.

Claim 20 has been rejected under 35 U.S.C. 102(e) as being anticipated by Santin, U.S. Pat. No. 6,847,574.

Claims 24-28 have been rejected under 35 U.S.C. 102(e) as being anticipated by Pekny, U.S. Pat. No. 6,553,510.

Applicant respectfully traverses these rejections because the cited references do not disclose or suggest every element of any claim, as the following analysis shows.

CLAIM 1

Regarding amended Claim 1, Pekny at least fails to teach "wherein the detecting is performed during an erase operation" as recited in amended Claim 1.

The Office Action dated 5/4/05 asserts that "the detection of a defective memory and replacement of the memory is done during an erase and programming operations." However, Pekny discloses a verify step that is separate from an erase step (See Pekny, FIG. 4, step 402 "erase" and step 404 "verify.") Further, Pekny discloses "the memory array block is erased and each memory cell in the block is read to verify that it has been properly erased." (See Pekny, Col. 4, lines 46-48). Thus, Pekny at least fails to teach "wherein the detecting is performed during an erase operation" as recited in amended Claim 1.

Accordingly, for at least the foregoing reasons, Pekny fails to teach the limitations of Claim 1. The rejection of Claim 1 is thus unsupported, and must be withdrawn. Claims 2-4 and 6-13 depend from allowable Claim 1 and are allowable for at least this reason.

CLAIM 14

Regarding amended Claim 14, Scheuerlein at least fails to teach "to monitor electrical characteristics in the plurality of accessible memory units during an erase operation" as recited in Claim 14.

Scheuerlein discloses a row redundancy method that is performed at the factory while a memory array is being tested, in particular a first short detection mode and a second short detection mode. The first short detection mode selects a row line and biases

the array such that column lines are at the same voltage as the selected row line. The second short detection mode selects a row line and biases the array such that the unselected and selected row lines are substantially less that the bias of the column lines. (See Scheuerlein, Column 7, lines 35-64.) Both the first and the second short detection modes as disclosed in Scheurlein are not performed during an erase operation.

Accordingly, for at least the foregoing reasons, Scheuerlein fails to teach the limitations of Claim 14. The rejection of Claim 14 is thus unsupported, and must be withdrawn. Claims 15-19 depend from allowable Claim 14 and are allowable for at least this reason.

CLAIM 20

Regarding Claim 20, Santin at least fails to teach "a failure detection unit coupled to the plurality of accessible memory units configured to monitor electrical characteristics in the plurality of accessible memory units and to detect a electrical characteristic that identifies a defect in one of the plurality of accessible memory units" as recited in Claim 20.

The Office Action dated 5/4/05 asserts that Santin discloses such a failure detection unit with reference to a disable circuit 202. The disable circuit of Santin disables a fuse circuit 204 if it detects that the fuse circuit is unreliable. See Santin, Col. 4, lines 51-54. The fuse circuit 204 is not "one of the plurality of accessible memory units." Further, Santin does monitoring electrical characteristics.

Accordingly, for at least the foregoing reasons, Santin fails to teach the limitations of Claim 20. The rejection of Claim 20 is thus unsupported, and must be withdrawn. Claims 21-23 depend from allowable Claim 20 and are allowable for at least this reason.

CLAIM 24

For similar reasons as argued with respect to Claim 1 above, with respect to amended Claim 24, Pekny at least fails to teach "wherein the electrical characteristic is detected during an erase operation" as recited in Claim 24.

Accordingly, for at least the foregoing reasons, Pekny fails to teach the limitations of Claim 24. The rejection of Claim 24 is thus unsupported, and must be withdrawn. Claims 25-26 and 28-31 depend from allowable Claim 24 and are allowable for at least this reason.

Conclusion

For the foregoing reasons, it is submitted that the application is in condition for allowance, and indication of allowance by the Examiner is respectfully requested. If the Examiner has any questions concerning this application, he or she is requested to telephone the undersigned at the telephone number shown below as soon as possible. If any fee insufficiency or overpayment is found, please charge any insufficiency or credit any overpayment to Deposit Account No. 02-2666.

Respectfully submitted,

Intel Corporation

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